Abstract of the Disclosure

Integrated circuit inductors may be formed using a spiral layout on the surface of an interconnect dielectric stack. Conductive lines from two or more metal layers in the interconnect stack may be electrically connected using one or more via trenches. The via trench interconnection arrangement reduces the resistance of the inductor and increases the inductor's Q-factor. The Q-factor of the inductor may also be increased by placing a region of n-type and p-type wells or a metal plate region beneath the inductor to reduce power losses during operation. Shallow trench isolation may be used to reduce eddy currents and increase Q. The effects of copper dishing and trench blow-out may be used during inductor fabrication. A dual damascene fabrication process may be used.